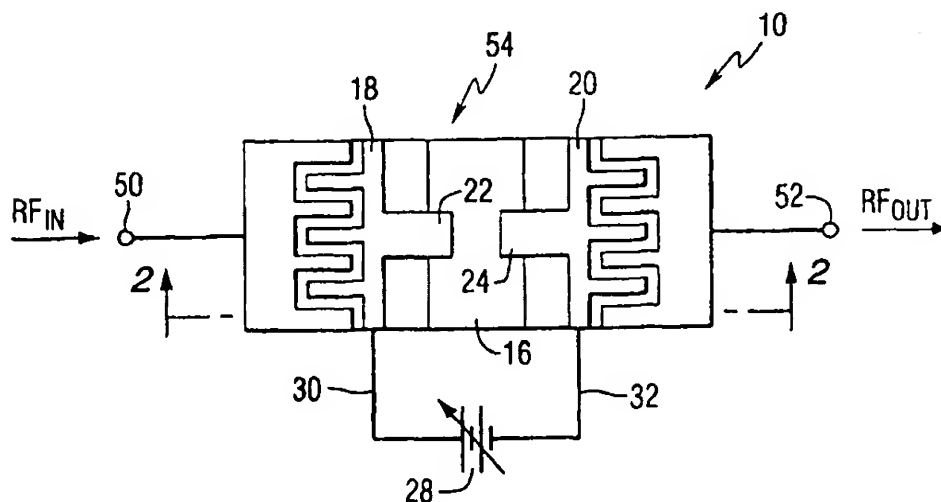




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/US99/26113 (22) International Filing Date: 4 November 1999 (04.11.99) (30) Priority Data: 60/107,684 9 November 1998 (09.11.98) US (71) Applicant: PARATEK MICROWAVE, INC. [US/US]; 6935-N Oakland Mills Road, Columbia, MD 21045 (US). (72) Inventors: SENGUPTA, Louise, C.; 12 New Haven Boulevard, Warwick, MD 21912 (US). STOWELL, Steven, C; 9525 Wandering Way, Columbia, MD 21045 (US). ZHU, Yongfei; Suite 6, 5275 Rivendell Lane, Columbia, MD 21044 (US). SENGUPTA, Somnath; 12 New Haven Boulevard, Warwick, MD 21912 (US). (74) Agent: LENART, Robert, P.; Eckert Seamans Cherin & Mellott, LLC, 44th floor, 600 Grant Street, Pittsburgh, PA 15219 (US).	(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).  Published With international search report.	

(54) Title: FERROELECTRIC VARACTOR WITH BUILT-IN DC BLOCKS



## (57) Abstract

A voltage tunable dielectric varactor includes a tunable ferroelectric layer and first and second non-tunable dielectric layers. First and second electrodes positioned adjacent to the tunable ferroelectric layer form a tunable capacitor. A third electrode is positioned adjacent to the first non-tunable dielectric layer such that the third and first electrodes and the first non-tunable dielectric layer form a first blocking capacitor. A fourth electrode is positioned adjacent to the second non-tunable dielectric layer such that the fourth and second electrodes and the second non-tunable dielectric layer form a second blocking capacitor.

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## FERROELECTRIC VARACTOR WITH BUILT-IN DC BLOCKS

### CROSS REFERENCE TO RELATED PATENT APPLICATION

This application claims the benefit of United States Provisional Patent Application No. 60/ 107,684, filed November 9, 1998.

### FIELD OF INVENTION

5           The present invention relates generally to voltage tunable varactors with associated DC blocking capacitors.

### BACKGROUND OF INVENTION

Varactors are voltage tunable capacitors in which the capacitance is dependent on a voltage applied thereto. This property can find applications in electrically tuning radio frequency (RF) circuits, such as filters, phase shifters, and so on. The most commonly used varactor is semiconductor diode varactor, which has the advantages of high tunability and low tuning voltage, but suffers low Q, low power handling capability, and limited capacitance range. A new type of varactor is a ferroelectric varactor in which the capacitance is tuned by varying the dielectric constant of a ferroelectric material by changing the bias voltage. Ferroelectric varactors have high Q, high power handling capacity, and high capacitance range.

10           15

One ferroelectric varactor is disclosed in United States Patent No. 5,640,042 entitled "Thin Film Ferroelectric Varactor" by Thomas E. Kosciwa et al. That patent discloses a planar ferroelectric varactor, which includes a carrier substrate layer, a high temperature superconducting metallic layer deposited on the substrate, a lattice matching, a thin film ferroelectric layer deposited on the metallic layer, and a plurality of metallic conductors disposed on the ferroelectric layer and in contact with radio frequency (RF) transmission lines in tuning devices. Another tunable capacitor using a ferroelectric element in combination with a superconducting element is

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disclosed in United States Patent No. 5,721,194. Tunable varactors that utilizes a ferroelectric layer, and various devices that include such varactors are also disclosed in United States Patent Application Serial No. \_\_\_\_\_, entitled "Voltage Tunable Varactors And Tunable Devices Including Such Varactors ", filed October 15, 1999, and assigned to the same assignee as the present invention.

When using such varactors in various devices, it is necessary to insert DC blocking capacitors in the RF transmission line to isolate the DC bias voltage from the other parts of RF system. These DC blocks on the transmission line may result in additional insertion loss to the RF system, and inconvenience in the design and construction of an RF system.

There is a need for varactors with reduced DC block insertion loss, but with high tunability, for use in the VHF, UHF, microwave and other tunable circuits, such as filters, phase shifters, voltage controlled oscillators and so on.

#### SUMMARY OF INVENTION

A voltage tunable dielectric varactor assembly constructed in accordance with this invention includes a tunable ferroelectric layer and first and second non-tunable dielectric layers. First and second electrodes positioned adjacent to the tunable ferroelectric layer form a tunable capacitor. The first and second electrodes are also positioned adjacent to the first and second non-tunable layers, respectively. A third electrode is positioned adjacent to the first non-tunable dielectric layer such that the third and first electrodes and the first non-tunable dielectric layer form a first blocking capacitor. A fourth electrode is positioned adjacent to the second non-tunable dielectric layer such that the fourth and second electrodes and the second non-tunable dielectric layer form a second blocking capacitor.

In one embodiment, the voltage tunable dielectric varactor includes a substrate having a generally planar surface and a tunable ferroelectric layer positioned on the generally planar surface of the substrate. First and second electrodes are positioned on a surface of the tunable ferroelectric layer opposite the generally planar surface of the substrate, with the first and second electrodes being separated to form a first gap. First and second non-tunable dielectric layers are also positioned on the generally planar surface of the substrate. A third electrode is positioned on the

surface of the first non-tunable dielectric layer opposite the generally planar surface of the substrate such that the third and first electrodes form a second gap. A fourth electrode is positioned on the surface of the second non-tunable dielectric layer opposite the generally planar surface of the substrate such that the fourth and second electrodes form a third gap.

In another embodiment, the voltage tunable dielectric varactor includes a tunable ferroelectric layer and first and second non-tunable dielectric layers. The tunable layer is positioned between first and second electrodes to form a tunable capacitor. The first non-tunable layer is positioned between the first electrode and a third electrode to form a first blocking capacitor. The second non-tunable layer is positioned between the second electrode and a fourth electrode to form a second blocking capacitor.

Ferroelectric varactor assemblies of the present invention can be used to produce a phase shift in various microwave devices, and in other devices such as tunable filters.

#### BRIEF DESCRIPTION OF THE DRAWINGS

A full understanding of the invention can be gained from the following description of the preferred embodiments when read in conjunction with the accompanying drawings in which:

FIG. 1 is a top view of a planar varactor assembly with built-in DC blocking capacitors constructed in accordance with the invention;

FIG. 2 is a cross sectional view of the varactor assembly of FIG. 1, taken along line 2-2;

FIG. 3 is an equivalent circuit of the varactor with built-in DC block capacitors of FIGs. 1 and 2;

FIG. 4 is a graph of the tunability versus capacitance ratio for a varactor assembly constructed in accordance with the invention

FIG. 5 is a top view of a varactor assembly with built-in DC blocking capacitors constructed in accordance with another embodiment of the invention;

FIG. 6 is a cross sectional view of the varactor assembly of FIG. 5, taken along line 6-6;

FIG. 7 is a top view of a varactor assembly with built-in DC blocking capacitors constructed in accordance with another embodiment of the invention; and

FIG. 8 is a cross sectional view of the varactor assembly of FIG. 7, taken along line 8-8.

#### 5 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, FIGs. 1 and 2 are top and cross sectional views of a varactor assembly 10 constructed in accordance with this invention.. The varactor assembly 10 includes a substrate 12 having a generally planar top surface 14. A tunable ferroelectric layer 16 is positioned adjacent to the top surface of the substrate. Metal electrodes 18 and 20 are positioned on top of the ferroelectric layer. The electrodes 18 and 20 are shaped to have projections 22 and 24. The ends of these projections form a gap 26 on the surface of the tunable ferroelectric layer. The combination of electrodes 18 and 20, and tunable ferroelectric layer 16 form a tunable capacitor 54. The capacitance of the tunable capacitor can be changed by applying a bias voltage to the electrodes 18 and 20.

In the preferred embodiment, the substrate 12 is comprised of a material having a relatively low permittivity such as MgO, Alumina,  $\text{LaAlO}_3$ , Sapphire, or a ceramic. For the purposes of this invention, a low permittivity is a permittivity of less than about 30. In the preferred embodiment, the tunable ferroelectric layer 16 is comprised of a material having a permittivity in a range from about 20 to about 2000, and having a tunability in the range from about 10% to about 80% at a bias voltage of about 10 V/ $\mu\text{m}$ . The tunable ferroelectric layer can be comprised of Barium-Strontium Titanate,  $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$  (BSTO), where x can range from zero to one, or BSTO-composite ceramics. Examples of such BSTO composites include, but are not limited to: BSTO-MgO, BSTO-MgAl<sub>2</sub>O<sub>4</sub>, BSTO-CaTiO<sub>3</sub>, BSTO-MgTiO<sub>3</sub>, BSTO-MgSrZrTiO<sub>6</sub>, and combinations thereof. The dielectric film of the ferroelectric capacitor may be deposited by screen printer, laser ablation, metal-organic solution deposition, sputtering, or chemical vapor deposition techniques. The tunable layer in one preferred embodiment has a dielectric permittivity greater than 100 when subjected to typical DC bias voltages, for example, voltages ranging from about 5 volts to about 300 volts. The gap width must be optimized to increase ratio of the maximum capacitance  $C_{\text{max}}$  to the minimum capacitance  $C_{\text{min}}$  ( $C_{\text{max}}/C_{\text{min}}$ ) and

increase the quality factor (Q) of the device. The width of this gap has the most influence on the varactor parameters. The optimal width, g, will be determined by the width at which the device has maximum  $C_{\max}/C_{\min}$  and minimal loss tangent.

A controllable voltage source 28 is connected by lines 30 and 32 to electrodes 18 and 20. This voltage source is used to supply a DC bias voltage to the ferroelectric layer, thereby controlling the permittivity of the layer. The varactor assembly further includes first and second non-tunable dielectric layers 34 and 36 positioned adjacent to the generally planar surface of the substrate 12 and on opposite sides of the tunable ferroelectric layer 16. Electrode 18 extends over a portion of the top surface of non-tunable material 34. Electrode 38 is positioned adjacent a top surface of non-tunable layer 34 such that a gap 40 is formed between electrodes 18 and 34. The combination of electrodes 18 and 34 and non-tunable layer 34 forms a first DC blocking capacitor 42. The varactor assembly also includes an RF input 30 and an RF output 32.

Electrode 44 is positioned adjacent a top surface of non-tunable layer 36 such that a gap 46 is formed between electrodes 20 and 44. The combination of electrodes 20 and 44 and non-tunable layer 36 forms a second DC blocking capacitor 48. The dielectric films of the DC blocking capacitors may be deposited by screen printer, laser ablation, metal-organic solution deposition, sputtering, or chemical vapor deposition techniques.

An RF input 50 is connected to electrode 38. An RF output 52 is connected to electrode 44. The RF input and output are connected to electrodes 38 and 44, respectively, by soldered or bonded connections. The non-tunable dielectric layers 34 and 36, in the DC blocking capacitors 42 and 48, are comprised of a high dielectric constant material, such as BSTO composite. The DC blocking capacitors 42 and 48 are electrically connected in series with the tunable capacitor 54 to isolate the DC bias from the outside of the varactor assembly 10. To increase the capacitance of the two DC blocking capacitors 42 and 48 the electrodes have an interdigital arrangement as shown in FIG. 1.

In the preferred embodiments, the varactors may use gap widths of 5-50  $\mu\text{m}$ . The thickness of the ferroelectric layer ranges from about 0.1  $\mu\text{m}$  to about 20  $\mu\text{m}$ . A sealant can be inserted into the gaps to increase breakdown voltage. The

sealant can be any non-conducting material with a high dielectric breakdown strength to allow the application of high voltage without arcing across the gap, for example, epoxy or polyurethane.

The equivalent circuit of the varactor assemblies of this invention is shown in FIG. 3. The circuit is comprised of a tunable capacitor  $C_1$  connected in series to two non-tunable DC block capacitors  $C_2$  have equal capacitance in this example. Therefore, the resultant capacitor  $C_t$  of the varactor assembly is expressed as

$$\frac{1}{C_t} = \frac{1}{C_1} + \frac{2}{C_2} \quad (1)$$

or,

$$\frac{C_t}{C_1} = \frac{1}{1 + \frac{2C_1}{C_2}} \quad (2)$$

Here  $C_1$  is the capacitance of tunable capacitor, and  $C_2$  is the capacitance of DC block capacitors. In the case of:

$$C_1 \ll C_2 \quad (3)$$

Equation (2) gives:

$$C_t \approx C_1 \quad (4)$$

the tunability of resultant capacitor is related to that of the capacitor  $C_1$ . The tunability,  $t$ , of material can be defined as

$$t = \frac{1}{\epsilon_r} \frac{d\epsilon_r}{dE} \quad (5)$$

where  $\epsilon_r$  is the dielectric constant of the material, and  $E$  is strength of applied field. In the case of a capacitor where tunable material is used, often the capacitance  $C$  of the capacitor varies linearly with the dielectric constant, that is:

$$C = a\epsilon_r \quad (6)$$

where  $a$  is a capacitor parameter constant related to the geometrical structure, such as area, thickness and so on. The tunability can then be expressed as:

$$t = \frac{1}{\epsilon_r} \frac{d\epsilon_r}{dE} = \frac{1}{C} \frac{dC}{dE} \quad (7)$$

If  $C_1$  is a tunable capacitor with tunability  $t_1$  and  $C_2$  is a non-tunable capacitor, the resultant tunability  $t_t$  of the varactor assembly can be obtained from Equation (1) and Equation (7)

$$\frac{t_t}{C_t} = \frac{t_1}{C_1} \quad (8)$$

5 Using Equation (2), Equation (8) can be rewritten so that:

$$\frac{t_t}{t_1} = \frac{C_t}{C_1} = \frac{1}{1 + \frac{2C_1}{C_2}} \quad (9)$$

here  $t_t$  is the resultant tunability of the varactor assembly. Equation (1) shows that:

$$C_t < C_1 \quad (10)$$

since both  $C_1$  and  $C_2$  are both positive numbers. Therefore, from Equation (9),

$$10 \quad t_t < t_1 \quad (11)$$

If the condition of Equation (3) is applied ( $C_1 \ll C_2$ ),

$$t_t \approx t_1 \quad (12)$$

FIG. 4 shows the relationship of Equation (9) graphically. For example, it can be seen that at:

$$15 \quad \frac{C_2}{C_1} = 20, \text{ we have } \frac{t_t}{t_1} = \frac{C_t}{C_1} = 0.91.$$

$$\text{and at } \frac{C_2}{C_1} = 40, \text{ we have } \frac{t_t}{t_1} = \frac{C_t}{C_1} = 0.95.$$

Therefore, if  $C_2 \gg C_1$ , the resultant capacitance  $C_t$  and tunability  $t_t$  are mostly determined by the tunable capacitor  $C_1$ . Very little additional insertion loss is incurred through the integration of the DC blocking capacitors in the present invention, since the capacitance of the DC blocking capacitors is much higher than the capacitance of the varactor portion of the assembly. The insertion loss of the varactor assembly of the present invention results primarily from the tunable ferroelectric capacitor and its connections, since the capacitance of the tunable ferroelectric capacitor is much smaller than that of DC blocking capacitors.

25 FIGs. 5 and 6 are top and cross sectional views of a varactor assembly 56 with planar capacitor structure. In FIGs. 5 and 6, a capacitor 58 is a tunable

parallel-plate capacitor with DC bias metallic layer electrodes 60 and 62, which have bias terminations 64 and 66, respectively. The tunable material 68 in the capacitor 58 may be BSTO-based or related materials in the styles of bulk, tape, or thin film. DC block capacitors 70 and 72 are parallel-plate capacitors, which are connected in series to the tunable capacitor 58, respectively. The dielectric material 74 and 76 used in capacitors 70 and 72 is non-tunable material with high dielectric constant in the styles of bulk, tape or film. The capacitance of the DC blocking capacitors 70 and 72 should be at least 20 times higher than that of the tunable capacitor 58 by properly selection of dielectric constant of the dielectric material and the thickness of the dielectric layers. Electrodes 78 and 80 of the varactor assembly 56 are connected to a radio frequency (RF) signal through terminals 82 and 84. In order to satisfy the condition of  $C_2 \gg C_1$  in Equation (3), higher dielectric constant and thinner non-tunable layers 74 and 76, compared to the tunable layer 68, are chosen for the DC blocking capacitors 70 and 72 to increase the capacitance.

FIGs. 7 and 8 show a third embodiment of a varactor assembly 86 constructed in accordance with the present invention. The structure of varactor assembly 86 is similar to that of varactor assembly 56. However, multilayer capacitors are used as the DC blocking capacitors in varactor assembly 86 to replace the single layer DC blocking capacitors in varactor assembly 56 to increase the capacitance. The dielectric materials in this structure may be tape, thin or thick films. In FIGs. 7 and 8, a capacitor 88 is a tunable capacitor with DC bias metallic layer electrodes 90 and 92, which have bias terminations 94 and 96, respectively. The tunable material 98 in the capacitor 88 may be BSTO-based or related materials. The multilayer DC blocking capacitors 100 and 102 are connected in series to the tunable capacitor 88, respectively. The dielectric material used in capacitors 100 and 102 is non-tunable material with a high dielectric constant. With this embodiment, the capacitance of the DC blocking capacitor 100 and 102 should be at least 40 times higher than that of the tunable capacitor 88 by proper selection of the dielectric material, the thickness of the dielectric layer, and the number of dielectric layers. Electrodes 104 and 106 of the varactor assembly 86 are connected to the RF transmission lines through the electrode terminations 108 and 110.

A ferroelectric varactor assembly with built-in DC block(s) has been described, in which low loss and high tunability materials are used. The built-in DC blocking capacitors make the varactor much easier to use in RF circuits, and eliminate the insertion loss caused by conventional DC blocking capacitors when conventional  
5 varactor is used. The low loss and high tunability materials may be Barium-strontium titanate,  $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$  (BSTO), where  $x$  is less than 1, or BSTO- based composites. These high quality materials may significantly improve the varactor performance of the present invention. The ferroelectric varactor may be made of bulk, thin film, or thick film ferroelectric materials.

10 Accordingly, the present invention, by utilizing built-in DC blocking capacitors and high quality tunable ferroelectric materials, provides a high performance of ferroelectric varactor assembly, elimination of conventional DC block insertion loss, and significant convenience for RF circuit design and processing. This invention has many practical applications and many other modifications of the  
15 disclosed devices may be obvious to those skilled in the art without departing from the spirit and scope of this invention as defined by the following claims.

What is claimed is:

1. A voltage tunable dielectric varactor assembly comprising:  
a tunable ferroelectric layer;  
first and second electrodes positioned adjacent to the tunable  
5 ferroelectric layer forming a tunable capacitor;  
a first non-tunable dielectric layer positioned adjacent to the first  
electrode;  
a third electrode positioned adjacent to the first non-tunable dielectric  
layer, said third and first electrodes and said first non-tunable dielectric layer forming  
10 a first blocking capacitor;  
a second non-tunable dielectric layer positioned adjacent to the second  
electrode; and  
a fourth electrode positioned adjacent to the second non-tunable  
dielectric layer, said fourth and second electrodes and said second non-tunable  
15 dielectric layer forming a second blocking capacitor.
2. A voltage tunable dielectric varactor assembly as recited in  
claim 1, wherein the capacitance between said first and second electrodes is less than  
the capacitance between said first and third electrodes by a factor of at least about 20.
3. A voltage tunable dielectric varactor assembly as recited in  
20 claim 1, wherein the tunable ferroelectric layer has a permittivity in a range from  
about 20 to about 2000, and a tunability in a range from about 10% to about 80% at a  
bias voltage of about 10 V/ $\mu\text{m}$ .
4. A voltage tunable dielectric varactor assembly as recited in  
claim 1, further comprising a substrate for supporting said tunable ferroelectric layer  
25 and said first and second non-tunable dielectric layers.

5. A voltage tunable dielectric varactor assembly as recited in claim 4, wherein the substrate comprises one of the group of: MgO, Alumina, LaAlO<sub>3</sub>, sapphire, and a ceramic.

6. A voltage tunable dielectric varactor assembly as recited in claim 1, wherein the tunable ferroelectric layer comprises one of:

- a tunable ferroelectric thick film;
- a tunable ferroelectric bulk ceramic; and
- a tunable ferroelectric thin film.

7. A voltage tunable dielectric varactor assembly comprising:  
a substrate having a generally planar surface;  
a tunable ferroelectric layer positioned on the generally planar surface of the substrate;

first and second electrodes positioned on a surface of the tunable ferroelectric layer opposite the generally planar surface of the substrate, said first and second electrodes being separated to form a gap therebetween;

first and second non-tunable dielectric layers positioned on the generally planar surface of the substrate, wherein a portion of the first non-tunable dielectric layer is positioned adjacent to the first electrode, and wherein a portion of the second non-tunable dielectric layer is positioned adjacent to the second electrode;

a third electrode positioned on a surface of the first non-tunable dielectric layer opposite the generally planar surface of the substrate, said third and first electrodes being separated to form a second gap therebetween; and

a fourth electrode positioned on a surface of the second non-tunable dielectric layer opposite the generally planar surface of the substrate, said fourth and second electrodes being separated to form a third gap therebetween.

8. A voltage tunable dielectric varactor assembly as recited in claim 7, wherein the capacitance between said first and second electrodes is less than the capacitance between said first and third electrodes by a factor of at least about 20.

9. A voltage tunable dielectric varactor assembly as recited in claim 7, wherein said second and third gaps are interdigital gaps.

10. A voltage tunable dielectric varactor assembly as recited in claim 7, wherein the tunable ferroelectric layer has a permittivity in a range from

about 20 to about 2000, and a tunability in a range from about 10% to about 80% at a bias voltage of about 10 V/ $\mu$ m.

11. A voltage tunable dielectric varactor assembly as recited in claim 7, wherein the substrate comprises one of the group of: MgO, Alumina,  
5 LaAlO<sub>3</sub>, sapphire, and a ceramic.

12. A voltage tunable dielectric varactor assembly as recited in claim 7, wherein the tunable ferroelectric layer comprises one of:

a tunable ferroelectric thick film;  
a tunable ferroelectric bulk ceramic; and  
10 a tunable ferroelectric thin film.

13. A voltage tunable dielectric varactor assembly as recited in claim 7, wherein the tunable ferroelectric includes an RF input and an RF output for passing an RF signal through the tunable ferroelectric layer in a first direction, and wherein the first gap extends in a second direction substantially perpendicular to the  
15 first direction.

14. A voltage tunable dielectric varactor assembly comprising:  
a tunable ferroelectric layer;  
first and second electrodes positioned on opposite sides of the tunable ferroelectric layer;

20 first and second non-tunable dielectric layers, wherein the first non-tunable layer is positioned adjacent to the first electrode and wherein the second non-tunable layer is positioned adjacent to the second electrode;

a third electrode positioned adjacent to a surface of the first non-tunable dielectric layer opposite the first electrode; and

25 a fourth electrode positioned adjacent to a surface of the second non-tunable dielectric layer opposite the second electrode.

15. A voltage tunable dielectric varactor assembly as recited in claim 14, wherein the capacitance between said first and second electrodes is less than the capacitance between said first and third electrodes by a factor of at least about 20.

30 16. A voltage tunable dielectric varactor assembly as recited in claim 14, wherein the tunable ferroelectric layer has a permittivity in a range from

about 20 to about 2000, and a tunability in a range from about 10% to about 80% at a bias voltage of about 10 V/ $\mu\text{m}$ .

17. A voltage tunable dielectric varactor assembly as recited in claim 14, wherein the tunable ferroelectric layer comprises one of:

- 5           a tunable ferroelectric thick film;  
            a tunable ferroelectric bulk ceramic; and  
            a tunable ferroelectric thin film.

18. A voltage tunable dielectric varactor assembly as recited in claim 14, further comprising:

- 10           a first plurality of additional non-tunable dielectric layers, wherein the third electrode is further positioned adjacent to a surface of each layer of the first plurality of additional non-tunable dielectric layers; and

- a second plurality of additional non-tunable dielectric layers, wherein the fourth electrode is further positioned adjacent to a surface of each layer of the  
15   second plurality of additional non-tunable dielectric layers.

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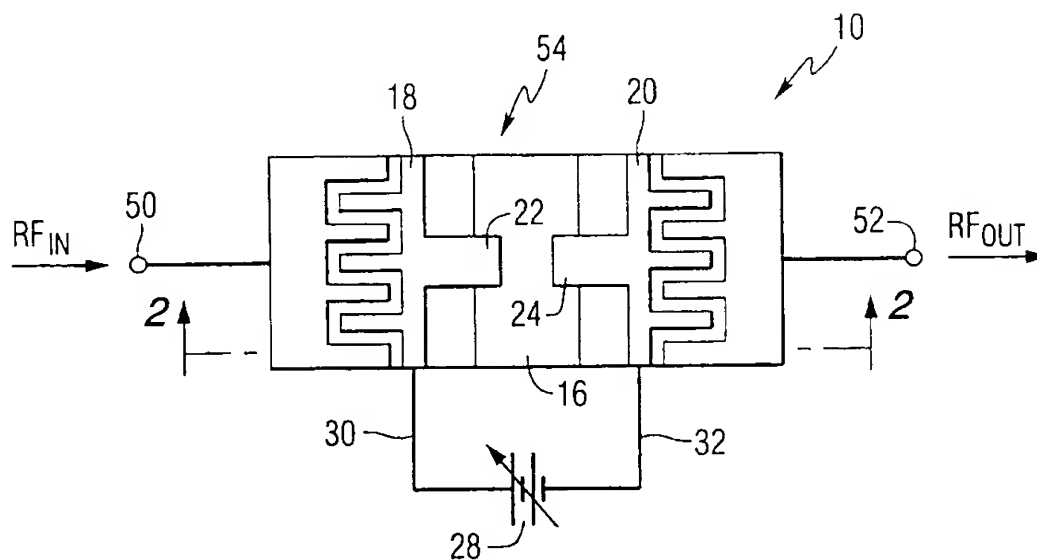


FIG. 1

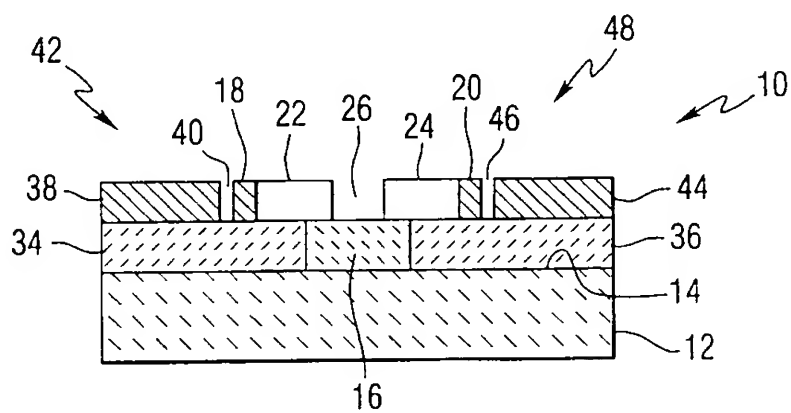


FIG. 2

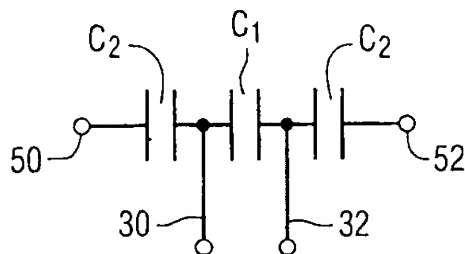


FIG. 3

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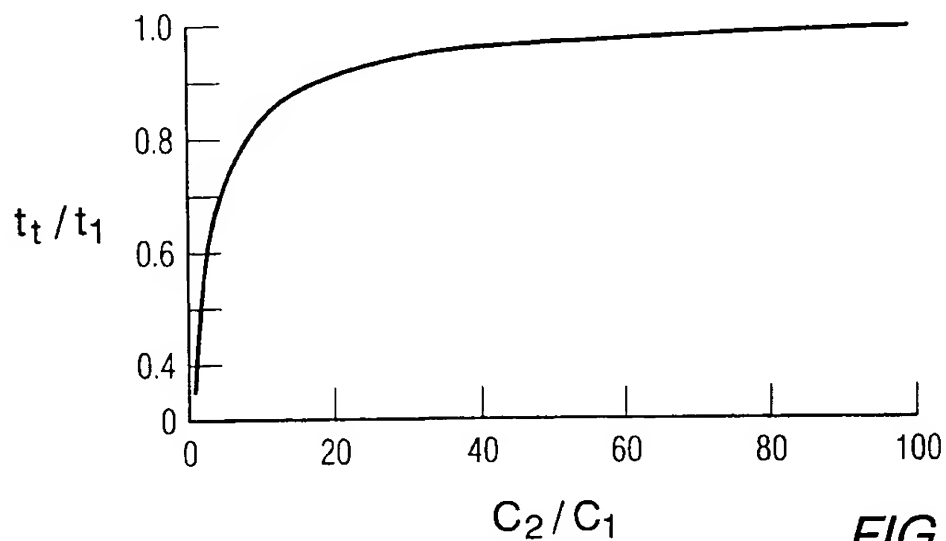


FIG. 4

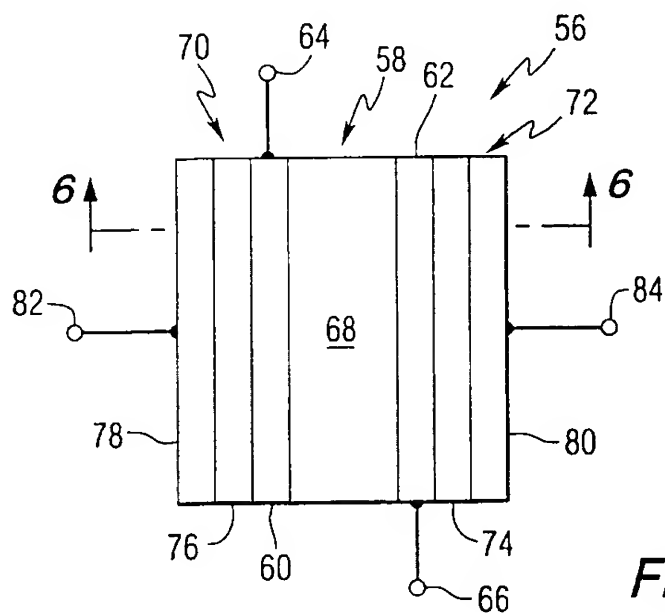


FIG. 5

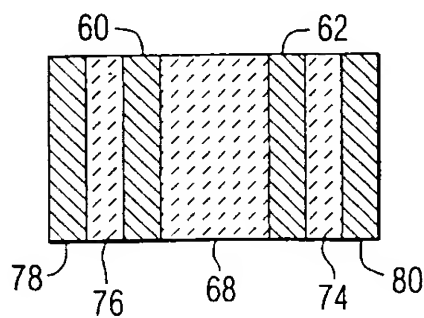


FIG. 6



# INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 99/26113

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 H01P1/18

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01P H01G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KOZYREV A ET AL: "FERROELECTRIC FILMS: NONLINEAR PROPERTIES AND APPLICATIONS IN MICROWAVE DEVICES" IEEE MTT-S INTERNATIONAL MICROWAVE SYMPOSIUM DIGEST, US, NEW YORK, NY: IEEE, 1998, pages 985-988, XP000822132 ISBN: 0-7803-4472-3 figure 1	1, 7, 14
A	US 5 745 335 A (WATT) 28 April 1998 (1998-04-28) column 3, line 50 - column 4, line 31; figure 1	1, 7, 14
A	EP 0 293 212 A (IWASAKI ELECTRIC CO., LTD.) 30 November 1988 (1988-11-30) column 4, line 18 - line 39; figures 4A, B	1, 7, 14
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

3 February 2000

Date of mailing of the international search report

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# INTERNATIONAL SEARCH REPORT

Inter. Patent Application No.

PCT/US 99/26113

## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	<p>WO 94 13028 A (SUPERCONDUCTING CORE TECHNOLOGIES, INC.)            9 June 1994 (1994-06-09)            page 24, line 17 -page 25, line 3            page 26, line 17 - line 20; figures 13,21            -----</p>	1,7,14

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Information on patent family members

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